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Fully Integrated Power Management: The Missing Link?

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***Abstract*—The integration level of electronic systems has continually increased over the past years, leading to significant reductions in cost, size and power consumption of consumer applications. One block, however, is still mostly implemented using discrete components: the Power Management Unit. This paper analyses the benefits of monolithic power management together with the main bottlenecks, and demonstrates how the latest research efforts in system- and circuit-level techniques pave the way for their wide-spread use.**

***Index Terms*—CMOS fully integrated power conversion, DC-DC converter, AC-DC converter, efficiency**

I. Introduction

Current electronic applications aim to be cheap, efficient and flexible. The power management unit however, plays a critical role in reaching these goals. As a System-On-Chip (SOC) for example uses multiple voltage rails or desires a flexible response to changing input- or output-power conditions, the power management unit should meet the same goals. Implementing the DC-DC or AC-DC power converter in an integrated CMOS technology holds many advantages, for which a cost and area decrease are the most remarkable. But, there is more.

This paper shows some techniques that elaborate the advantages of integrated power converters even more. The recurrent theme in this paper is *"efficiency"*. After all, a highly efficient power management unit results in large energy savings, a high power density, and this way a more compact implementation. On the other hand, efficient designs cannot be taken for granted. Keeping, for example, a DC-DC converter's efficiency high while the battery voltage is decreasing is a big challenge. As this problem calls for a converter with multiple conversion ratio's, so does the two-quadrant power supply that is addressed here. Looking at switched capacitor DC-DC converters, the losses contained in charging and discharging capacitors however do not change by using new converter topologies. Large energy savings are possible concerning this topic, as will be elaborated in this text.

This paper describes some recent techniques towards integrated DC-DC and AC-DC conversion as follows. Section II discusses the folding Dickson Converter as a way to convert a wide range DC input voltage. Powering serial loads is addressed in Section III by the two-quadrant switched capacitor converter. Hereafter, Section IV discusses how the efficiency of switched capacitor converters can be increased with advanced multiphasing techniques. As a contrast Section V describes the challenges towards monolithic AC-DC conversion. Finally, Section VI draws a conclusion.

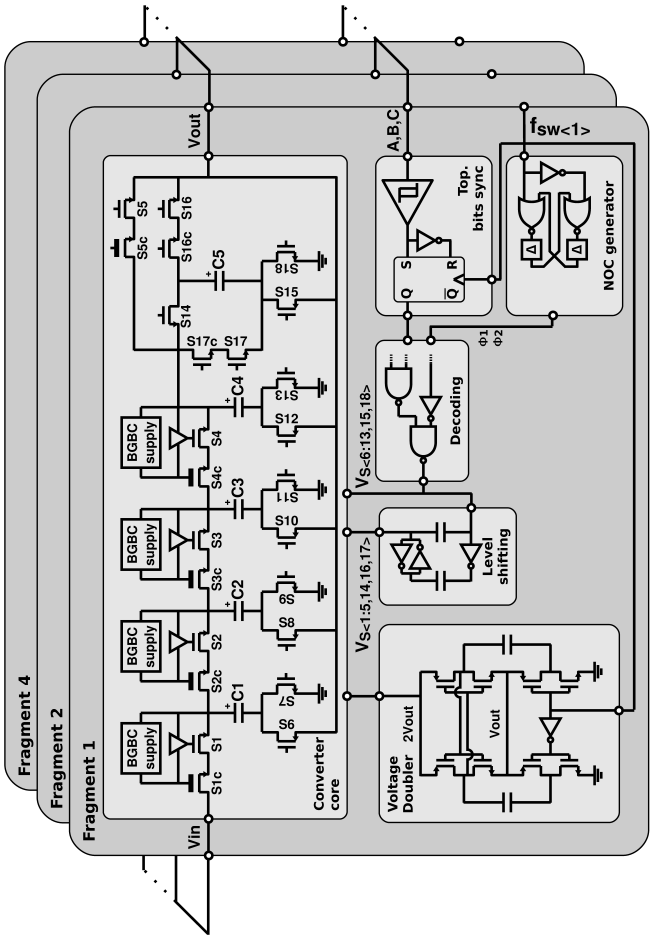

Fig. 1. System overview of the improved folding Dickson converter.

II. Wide Input Range SC Converters

Having switched capacitor (SC) DC-DC converters operate over a wide input voltage range is not a trivial task. The theoretical limit of SC converter efficiency, which is dependent on input and output voltage, usually limits the viable range. This can be solved by implementing several SC topologies

within the same converter, yet each topology imposes its limits, which makes this a strenuous task.

As a solution to this problem, the folding Dickson converter has been proposed. Thanks to its very regular structure, it can emulate several Voltage Conversion Ratios (VCR) by simply changing the phases of the switches, by which it lumps together two or more flying capacitors. The results of the first prototype have been discussed in [1], and showed the efficiency could benefit greatly from additional VCRs, especially in between VCR 2:1 and 3:1.

As such, a second prototype which tried to tackle this exact problem was designed [2], as shown in Fig. 1. An additional power stage was included, consisting of capacitor C5 and five power switches S14-S18, which expanded the amount of topologies from four to eight, leaving the operation of the folding Dickson topology unhampered. The plot of Fig. 2 highlights the efficiency of the improved folding Dickson converter at a maximum power density of $13.3\,\mathrm{mW/mm^2}$. The additional $\frac{2}{x}$-topologies drastically improve the efficiency in between the $\frac{1}{x}$-topologies, while other improvements, such as an improved well-biasing strategy, allow the converter to maintain efficiencies of 71% at step-down ratios. Furthermore, the high amount of VCRs smoothen the input current over the intended input voltage range.

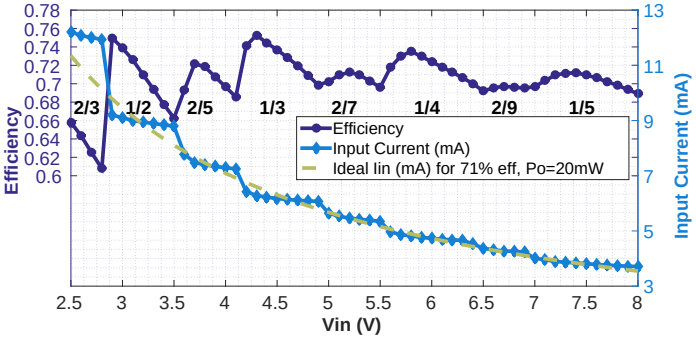

Fig. 2. Efficiency and input current of the second prototype.

III. Two-quadrant SC Converters for Vertically Stacked Voltage Domains

While on-chip DC-DC converters usually supply power to one or more loads in parallel, power-hungry loads are starting to push the boundaries of what is feasible, running into the so-called power wall [3], as ever higher power densities are required. However, if loads were to be stacked in series, as in Fig. 3, an interesting opportunity arises. The DC-DC converter needs to supply only the difference in current consumed by the loads, which can be substantially lower than previously. This however means that a two-quadrant power supply is required: one that can both source and sink current.

As it turns out, research in the field of two-quadrant SC converters has failed to grasp what this implies for the converter in question [4], [5]. As has been extensively discussed in [6], a converter is needed with at least two VCRs (in the case of constant load voltages): one to compensate the voltage drop

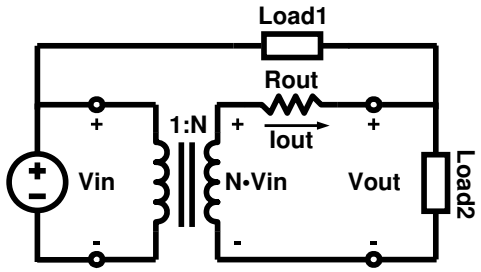

Fig. 3. Switched Capacitor DC-DC converter model, supplying two vertically stacked loads.

over the output impedance R_{out} when the converter is sourcing current, and one VCR to compensate the voltage drop when the converter is sinking current. An example of this is shown in Fig. 4, where $R_{load,2} = 100\Omega$, and R_{load1} is swept. The load lines plotted in this figure show that a valid operating point exists over the entire load range, by choosing the correct VCR. When loads are equal, the DC-DC converter will be practically idle, and very high efficiencies can be achieved, close to 100%, which will only be limited by the power consumption of the control loop.

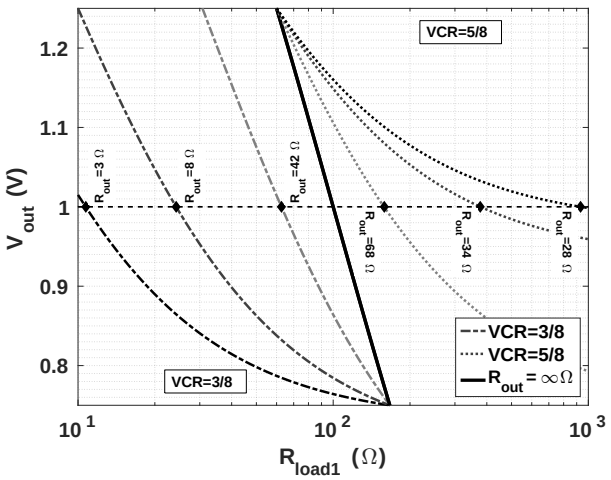

Fig. 4. Load line representation of a two-quadrant SC DC-DC converter with VCRs 8:5 and 8:3.

IV. Advanced Multiphasing SC Converters

Fully-integrated switched-capacitor (SC) converters have seen a great increase in popularity in recent years [7], and have been used for a wide range of applications. For some applications, though, regular converters are unable to deliver the necessary performance. This is due to the inherent challenges of the monolithic environment. The capacitance density of common technologies is quite limited which in turn limits the power density these converters can achieve. At the same time the maximum obtainable efficiency is constraint by the large parasitic substrate coupling [8].

As a solution, the concept of Advanced Multiphasing is proposed [9]–[11]. Here, the benefits of monolithic CMOS processes, including low complexity cost, high frequency ceiling and low fragmentation overhead, are used to overcome their major limitations.

A. Scalable Parasitic Charge Redistribution

A first advanced multiphasing technique, called scalable parasitic charge redistribution (SPCR), is introduced in [9], [10]. SPCR focuses on reducing a converter's parasitic coupling, or bottom-plate (BP), losses and thereby enables higher efficiencies than previously deemed possible.

Figure 5 shows the basic working principle for an 8 core SC converter. Rather than continuously switching each core between the high- and the low-voltage state, an extra state is introduced where the charge on the BP node is recycled from cores that make a high-to-low transition to cores that make the opposite transition. Moreover, this recycling happens in multiple charge redistribution steps (CRS). The higher the number of CRS, the larger the reduction of BP losses. A realization of the technique in a 40nm CMOS technology, reduces the BP losses by a factor of 10, leading to a record monolithic efficiency of 94.6%.

In addition, SPCR can create multiple additional DC voltage rails spread out evenly across the flying capacitor's BP node's swing, each of which can source or sink current [12]. As such, SPCR can also be thought of as a multiple-input-multiple-output (MIMO) DC-DC converter that uses only parasitic capacitance.

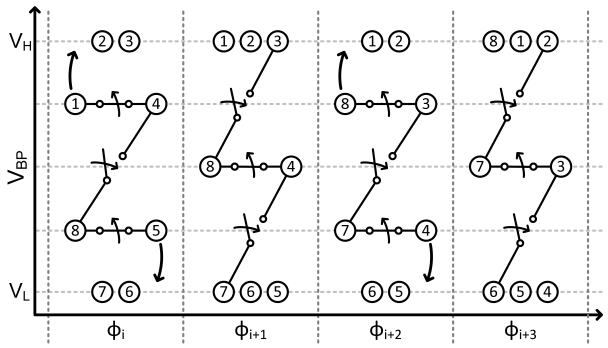

Fig. 5. Working principle of SPCR technique using 8 phase-shifted cores and 3 charge redistribution steps. Each labeled circle represents a different converter core. Arrows represent actions during phase transition. V_{BP} is the core's bottom-plate (BP) voltage.

B. Stage Outphasing and Multiphase Soft-Charging

Instead of reducing BP losses, it is also possible to reduce a converter's charge-sharing losses which is equivalent to an increase in its effective capacitance density. In Fig. 6, the techniques of stage outphasing (SO) and multiphase soft-charging (MSC) are shown for a Dickson converter [11].

With SO, each stage is split into two cells of equal size that run in anti phase and connect to the same intermediate nodes (k). Adjacent stages are furthermore shifted in phase relative to each other. As a result, each cell connects to two

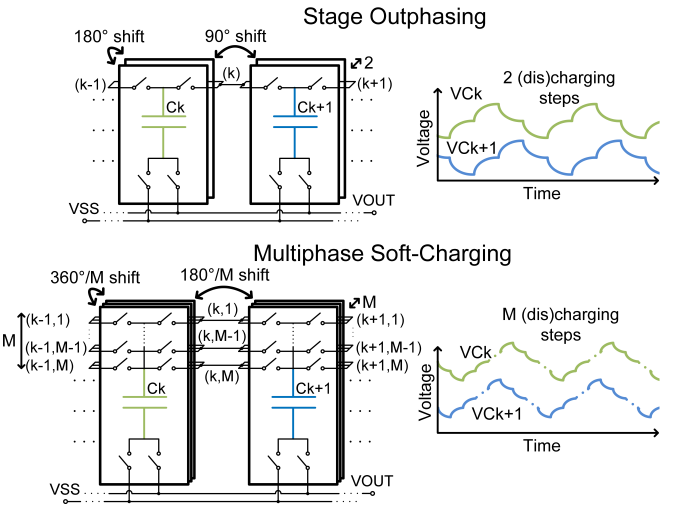

Fig. 6. Working principle of Dickson converter stages using stage outphasing and multiphase soft-charging.

cells of the adjacent stage over a full (dis)charge. For the same total charge transferred, the charge-sharing losses are halved.

MSC is a scalable technique where the intermediate nodes are split into multiple nodes $(k, 1)$ to (k, M). When the discharging and charging cells connect to these nodes in opposite order of each other, the node voltages will converge to M evenly spaced voltages. As such, each (dis)charge is spread over M steps, leading to an Mx improvement.

Even though in a full converter, some charge transfers can not be soft-charged by SO or MSC, the Dickson converter only has a minimum number of such transfers, making it an excellent candidate to use these techniques with. In [11], SO and MSC are combined to realize a fully-integrated 3:1 converter with 60% higher effective flying capacitance that achieves 82% efficiency at a power density of 1.1 $\mathrm{W/mm^2}$.

V. Integrated AC/DC Conversion

Aiming for a fully integrated DC-DC converter holds strong advantages for the power converter, as has been justified in [13]. A comparable reasoning is possible for AC-DC converters. Due to its wide availability, the AC-mains is the ideal source to power electronic applications. Nevertheless, the efficiency of available AC-DC converters drops strongly when decreasing the output power from the W-range to the μW- or mW-range. This way, low power applications and sensor nodes such as a wide variety of IoT-devices can benefit from a highly efficient fully integrated AC-DC conversion. The converter will benefit from a volume as well as a cost decrease while the efficiency can be high for the intended power-range.

On the other hand, one can state 3 main challenges for fully integrated converters powered from the AC-mains:

- The voltage ratings of standard CMOS components are typically limited to a few volts. This means that the high mains voltage ($110V_{RMS}$ or $230V_{RMS}$) should be

reduced such that the active on-chip components are protected from the high voltages. To limit cost, special technologies should be avoided in this context.
- A high efficiency with low losses and high power density is desired to keep cost and volume low.
- A high output power range is desired for the integrated converter such that applications with different power ratings can use the same converter. Otherwise, each application would need a customized power management unit. This increases process as well as design costs.

Traditionally, the high voltage compatibility is realized through special and bulky discrete components. Also, integrated passives can tolerate high voltages when customized. This way, an efficient magnetic transformer fits to transform the high mains into a lower AC-voltage. Nevertheless, it is difficult to integrate coils, resulting in a low power density and high cost. Even a resistive division can fit for the job, but the resulting power loss and heat production cannot be tolerated. This is why a capacitive approach is used in [14] and [15].

A customized capacitor separates the high AC-voltage from the active components in [14] and [15]. For a US mains input, [14] reports a power density of 1.06 $\mu\mathrm{W}/\mathrm{mm}^2$, which is higher than the amount reported in [15]. Due to a larger conduction time of the diodes in the rectifier circuit, it was possible to increase the output power in [14]. On the other hand, the capacitive approach puts a constraint on the available power density. First of all the integrable amount of high voltage tolerant capacitance is limited by the available chip-area. Secondly, the low mains frequencies imply that a capacitor is seen as a high impedant element, which constrains the output current. Combining both constraints results in a limited output power for a certain area. This way, increasing the power density as well as the output power range can be seen as challenges for future integrated AC-DC power converters.

VI. Conclusion

This paper gave an overview of the ongoing research concerning integrated power conversion. As the advantages of monolithic integration for power conversion have already been proven, this paper showed some advanced techniques towards wide input range DC-DC converters, like the folding Dickson converter achieving an efficiency of 71%, and the two-quadrant operation of a power unit. The intrinsic capacitive charging losses of SC DC-DC converters have been tackled by advanced multiphasing techniques reaching efficiencies of 94.6% and 82% for scalable parasitic charge redistribution and multiphase soft-charging respectively. As monolithic integration not only holds advantages for DC-DC conversion, large improvements are possible concerning AC-DC conversion efficiency and power density.

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